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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/544,801	04/07/2000	Shenpei Yamazaki	SEL 174	1717

7590 04/08/2004

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EXAMINER	
ERDEM, FAZLI	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/544,801	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Fazli Erdem	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27 and 64-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-27,68-71 and 76-79* is/are allowed.

6)☒ Claim(s) *1,3,4,6,8,9,64-67 and 72-75* is/are rejected.

7)☒ Claim(s) *2,5 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 10-27, 68-71 and 76-79 allowed

2. Claims 2, 5, 7 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 4, 6, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka et al. (6,504,215) in view of Kobayashi et al. (6,146,930) further in view of Abe et al. (JP 09260629).

Regarding Claims 1, 3, 4, 6, 8, and 9, Yamanaka et al. disclose an electro-optical apparatus having a display section and a peripheral driving circuit section where a single crystal silicon is graphoepitaxially grown using a step formed on a substrate as a seed by a catalyst process, and the obtained single crystal silicon layer is used for a dual gate type MOSTFT in an electro-optical apparatus such as a display section of a peripheral driving circuit integration type LCD. A single crystal silicon thin film having high electron/hole mobility is formed into a uniform film at a relatively low temperature which enables the manufacturing of an active matrix substrate incorporated with a high performance driver which can be used in a TFT display.

Yamanaka et al. do not show the required gate wiring structure. However, Kobayashi et al. disclose a method of fabricating an active-matrix liquid crystal display where an active-matrix liquid crystal display integrally formed with a driver circuit including a pair of substrates disposed in opposing relation to each other and a liquid crystal material sandwiched between the pair of substrates. Furthermore, Kobayashi et al. disclose the required gate wiring structure.

Yamanaka et al. and Kobayashi et al. combination fail to disclose the required connection structure outside the channel-forming region. However, Abe et al. disclose a manufacture of amplified solid-state element where the required connection structure outside the channel-forming region is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required connection structure in the required manner structure in Yamanaka et al. and Kobayashi et al. combination as taught by Abe et al. in order to have an LCD device with higher performance.

4. Claims 64, 66, 67, 72, 74 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seo (6,323,068) in view of Kobayashi et al. (5,767,930) further in view of Abe et al. (JP 09260629).

Regarding Claims 64, 66, 67, 72, 74 and 75, Seo discloses a liquid crystal display device integrated with driving circuit and method for fabricating the same where a method is provided for fabricating an LCD device integrated with a driver circuit on a substrate. A surface of the substrate is divided into a p-channel region, an n-channel region, and a pixel region. The method includes the steps of forming a gate electrode on each of the p-channel and n-channel, and pixel

regions of the substrate, forming a gate insulating layer on the entire surface of the substrate including the gate electrodes, forming a first transparent electrode layer over the gate insulating layer, forming a conductive layer over the first transparent electrode layer, forming a second transparent electrode layer over the conductive layer, removing portions of the first transparent electrode layer, the conductive layer and the second transparent electrode layer for form source/drain electrodes adjacent the gate electrodes in each of the p-channel, n-channel, and pixel regions of the substrate, doping first impurities into the second transparent electrode layer in the p-channel region, doping second impurities into the second transparent electrode layer in the n-channel region and in the pixel region, forming a semiconductor layer over the entire surface of the substrate, annealing the semiconductor layer, forming a passivation layer over the entire surface of the substrate and removing portions of the passivation layer, the second transparent electrode, and the conductive layer in the pixel region to expose a portion of the first transparent electrode layer. Seo does not disclose the required gate wiring structure. However, Kobayashi et al. disclose an active matrix liquid crystal display and fabrication method where the gate wiring structure is shown.

Seo and Kobayashi et al. combination fail to disclose the required connection structure outside the channel-forming region. However, Abe et al. disclose a manufacture of amplified solid-state element where the required connection structure is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required connection structure in the required manner structure in Seo and Kobayashi et al. combination as taught by Abe et al. in order to have an LCD device with higher performance.

5. Claim 65 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seo (6,323,068) in view of Kobayashi et al. (5,767,930) further in view of Iwanaga et al. (6,150,692) further in view of Abe et al. (JP 09260629).

Regarding Claim 65, Seo and Kobayashi combination disclose all the claimed subject matter except they fail to show the required conductive structure. However, Iwanaga et al. disclose a thin film semiconductor device for active matrix panel where the required conductive structure is shown.

Seo, Kobayashi et al., and Iwanaga et al. combination fail to disclose the required connection structure outside the channel forming region. However, Abe et al. disclose a manufacture of amplified solid-state element where the required connection structure is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required connection structure in the required manner structure in Seo, Kobayashi et al., and Iwanaga et al. combination as taught by Abe et al. in order to have an LCD device with higher performance.

6. Claim 73 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seo (6,323,068) in view of Kobayashi et al. (5,767,930) further in view of Sasano et al. (5,671,027) further in view of Abe et al. (JP 09260629).

Regarding Claims 73 and 77, Seo and Kobayashi combination disclose all the claimed subject matter except they fail to show the required conductive structure. However, Sasano et al.

disclose a thin film semiconductor device for active matrix panel where the required conductive structure is shown.

Seo, Kobayashi et al., and Sasano et al. combination fail to disclose the required connection structure outside the channel forming region. However, Abe et al. disclose a manufacture of amplified solid-state element where the required connection structure is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required connection structure in the required manner structure in Seo, Kobayashi et al. and Sasano et al. combination as taught by Abe et al. in order to have an LCD device with higher performance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (571) 272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915 The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

FE
April 4, 2004

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800